Fig.1

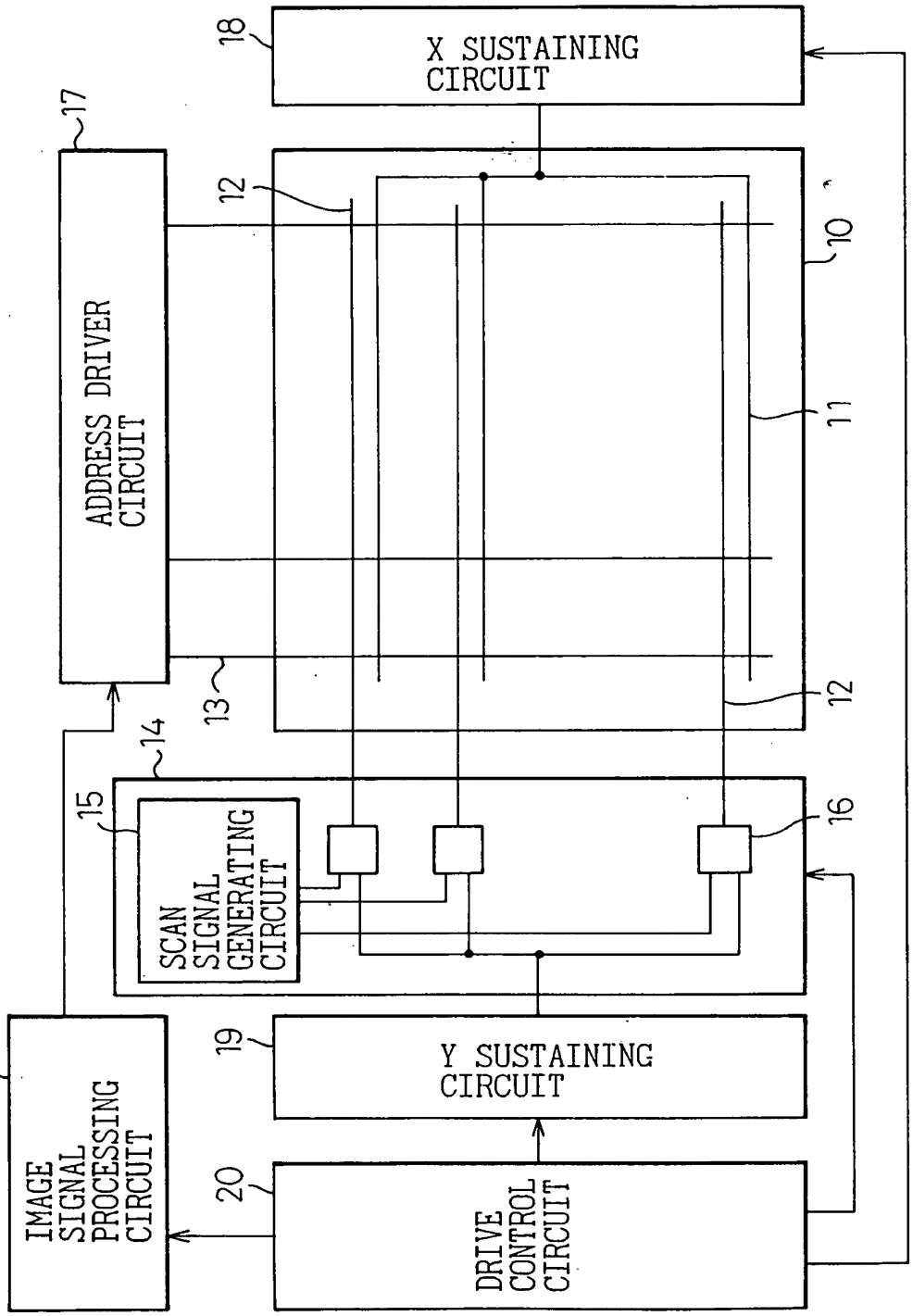

18
X SUSTAINING CIRCUIT
17
ADDRESS DRIVER CIRCUIT
12
10
11
12
13
14
15
SCAN SIGNAL GENERATING CIRCUIT
16
21
IMAGE SIGNAL PROCESSING CIRCUIT
19
Y SUSTAINING CIRCUIT
20
DRIVE CONTROL CIRCUIT

Fig.2

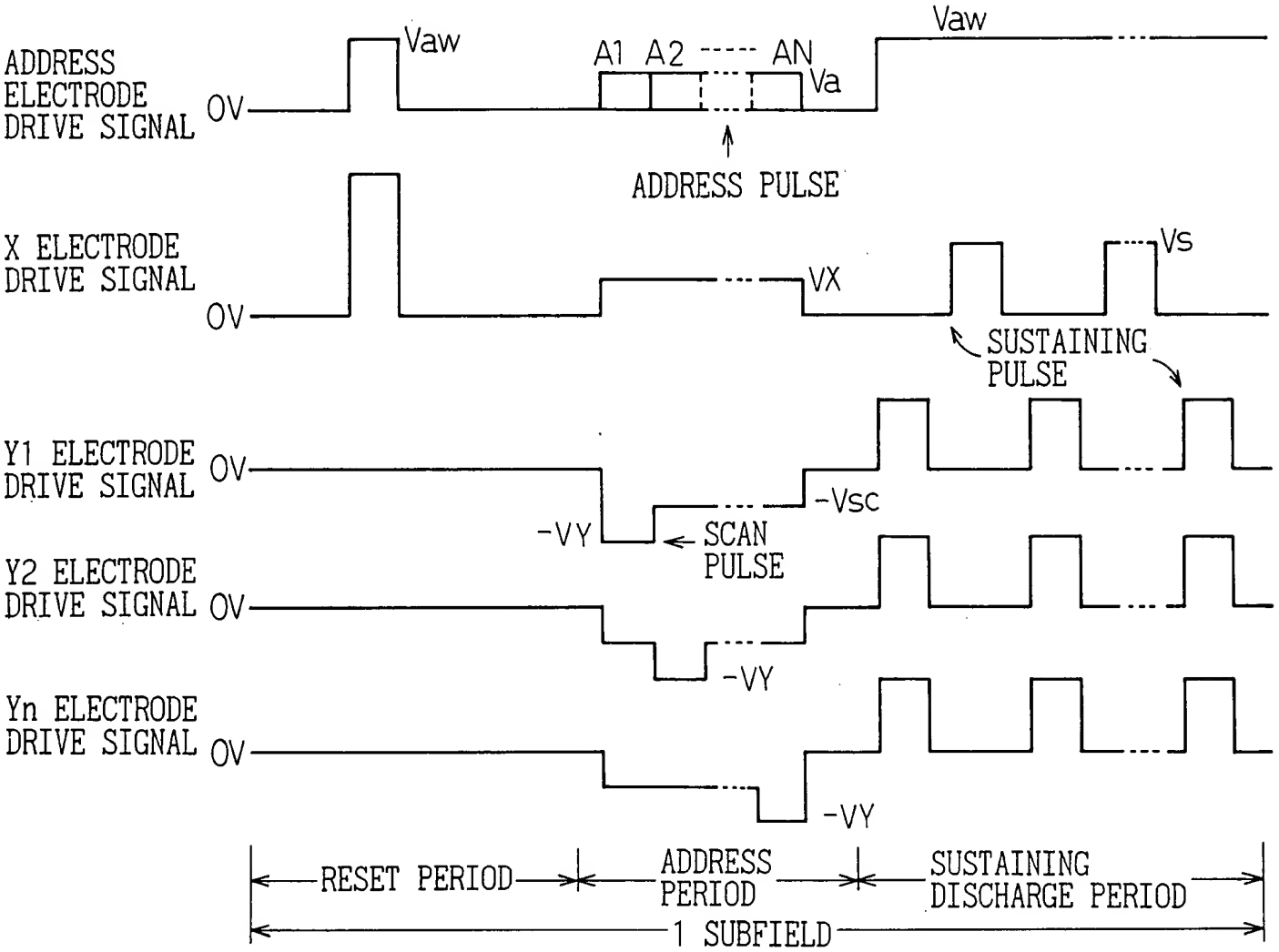


Fig.3

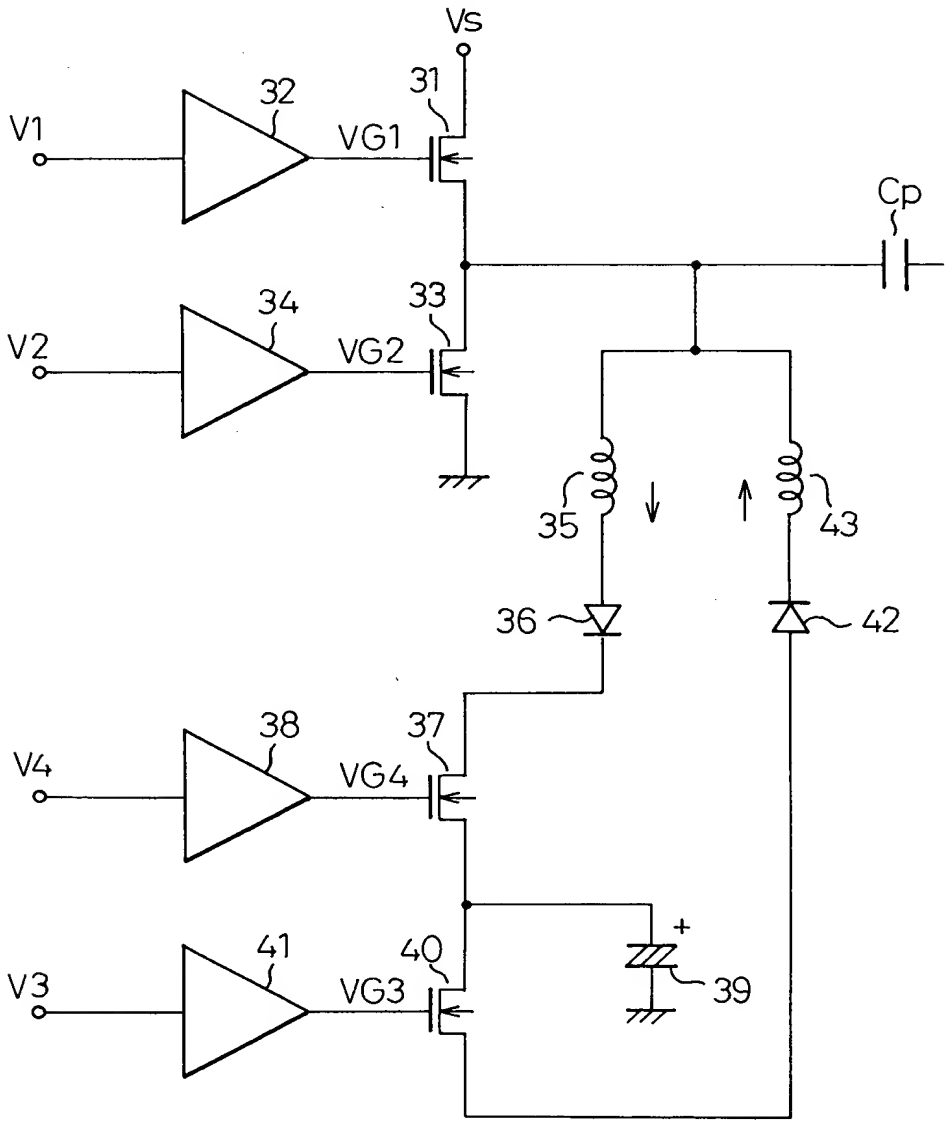

Vs
31
32
V1
VG1
Cp
33
34
V2
VG2
35
43
36
42
37
38
V4
VG4
+
39
40
41
V3
VG3

Fig.4

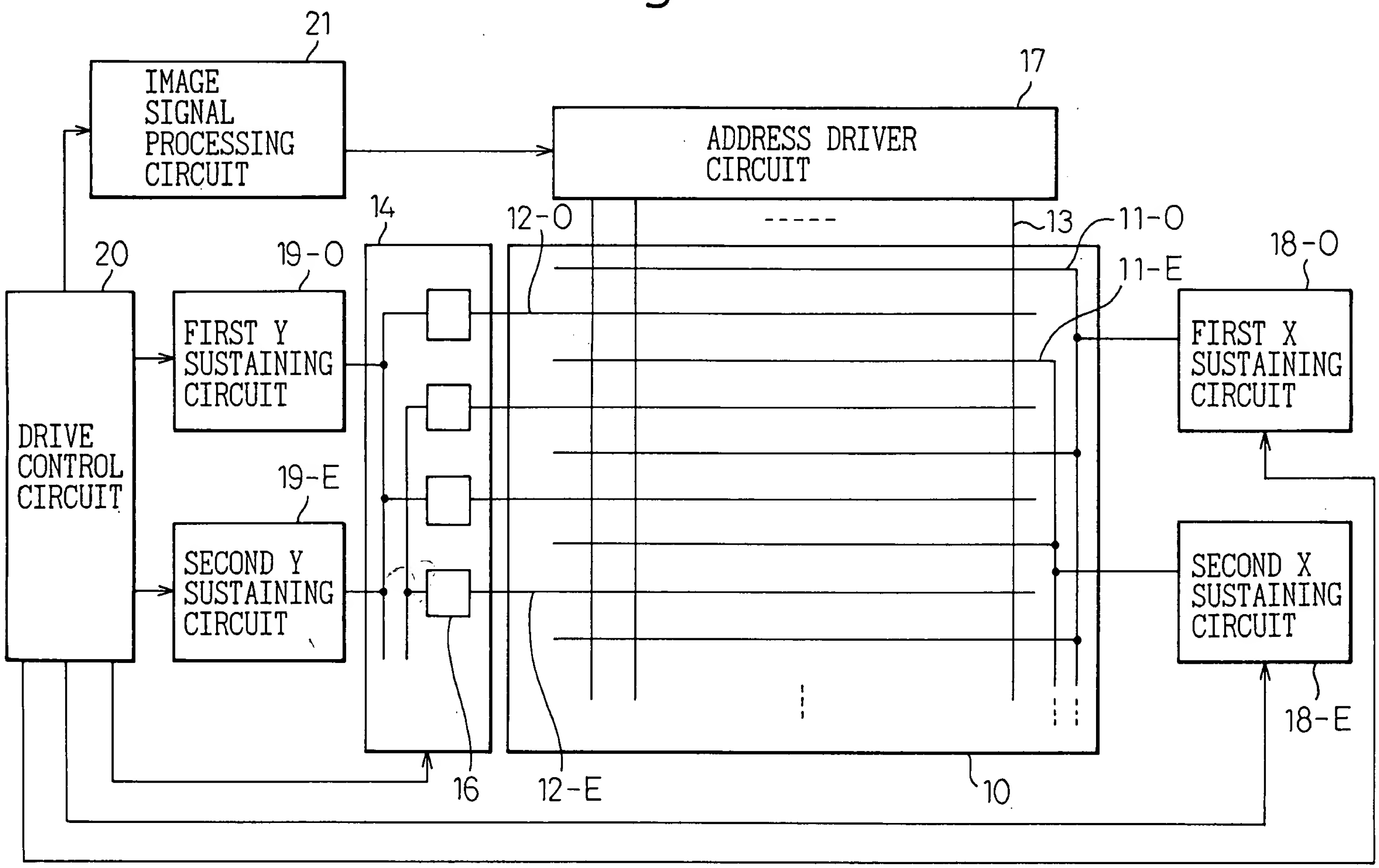

21
IMAGE SIGNAL PROCESSING CIRCUIT
17
ADDRESS DRIVER CIRCUIT
20
DRIVE CONTROL CIRCUIT
19-O
FIRST Y SUSTAINING CIRCUIT
19-E
SECOND Y SUSTAINING CIRCUIT
14
12-O
13
11-O
11-E
18-O
FIRST X SUSTAINING CIRCUIT
SECOND X SUSTAINING CIRCUIT
18-E
16
12-E
10

Fig.5A

ODD FIELD

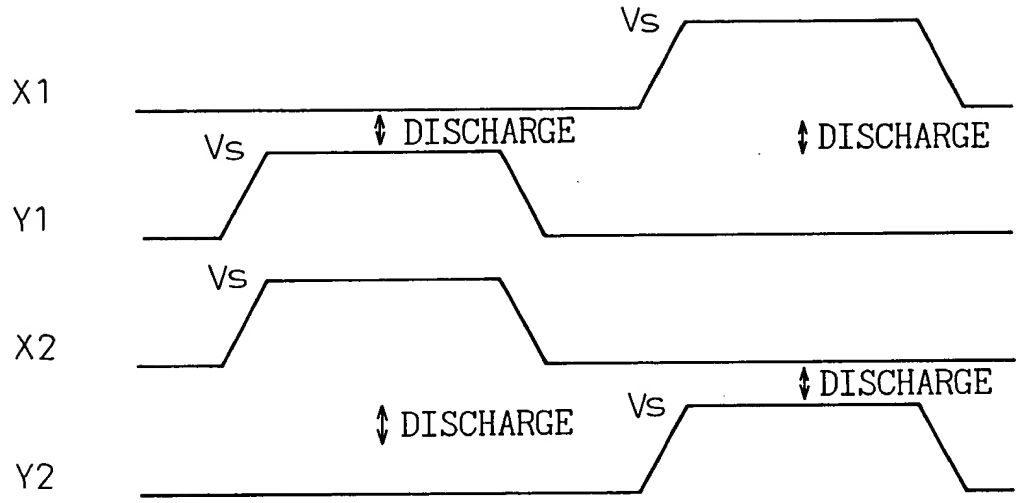


Fig.5B

EVEN FIELD

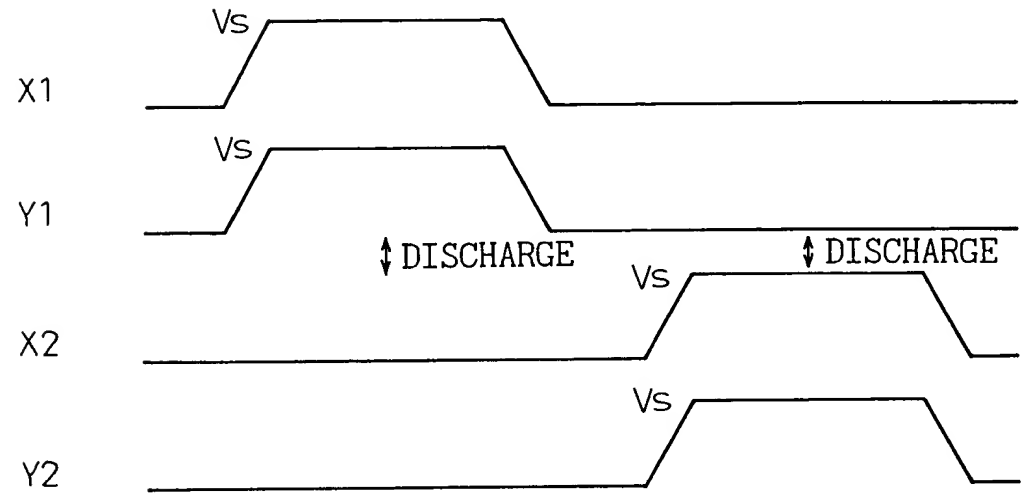


Fig.6A

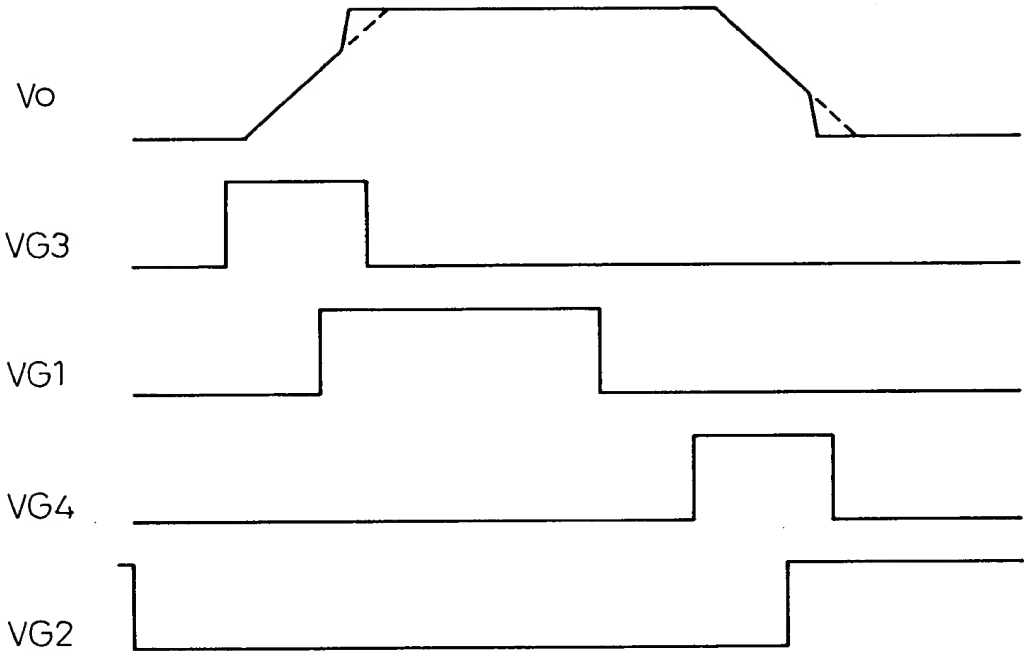


Fig.6B

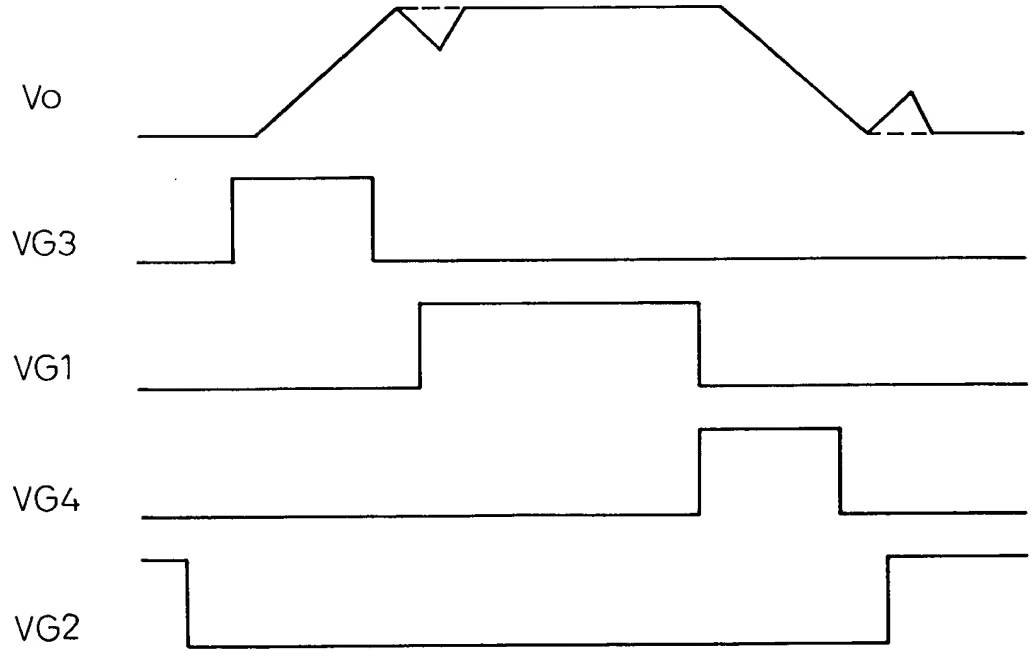


Fig.7

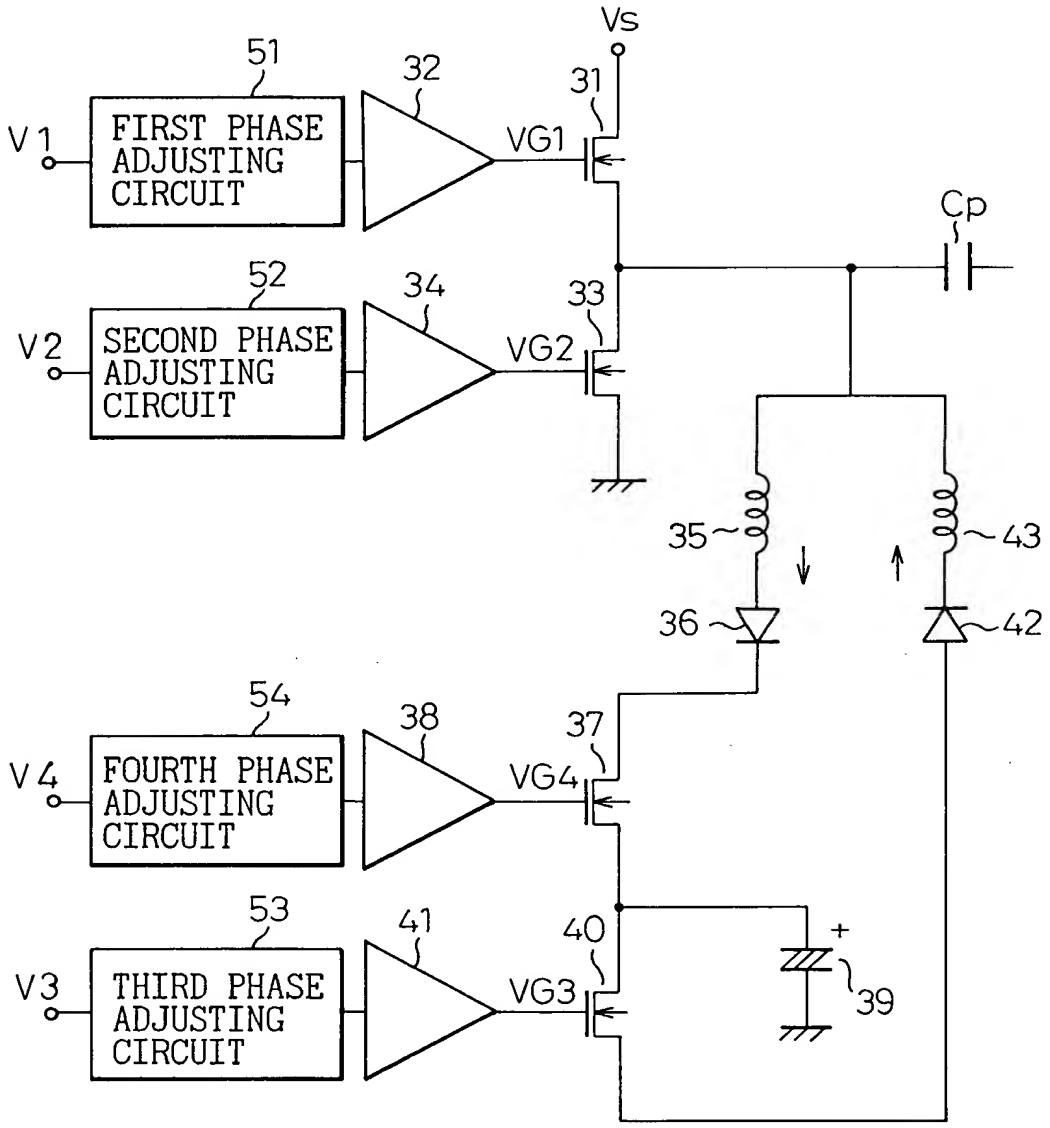

Vs
51
32
31
V1
FIRST PHASE ADJUSTING CIRCUIT
VG1
Cp
52
34
33
V2
SECOND PHASE ADJUSTING CIRCUIT
VG2
35
43
36
42
54
38
37
V4
FOURTH PHASE ADJUSTING CIRCUIT
VG4
53
41
40
+
V3
THIRD PHASE ADJUSTING CIRCUIT
VG3
39

Fig.8

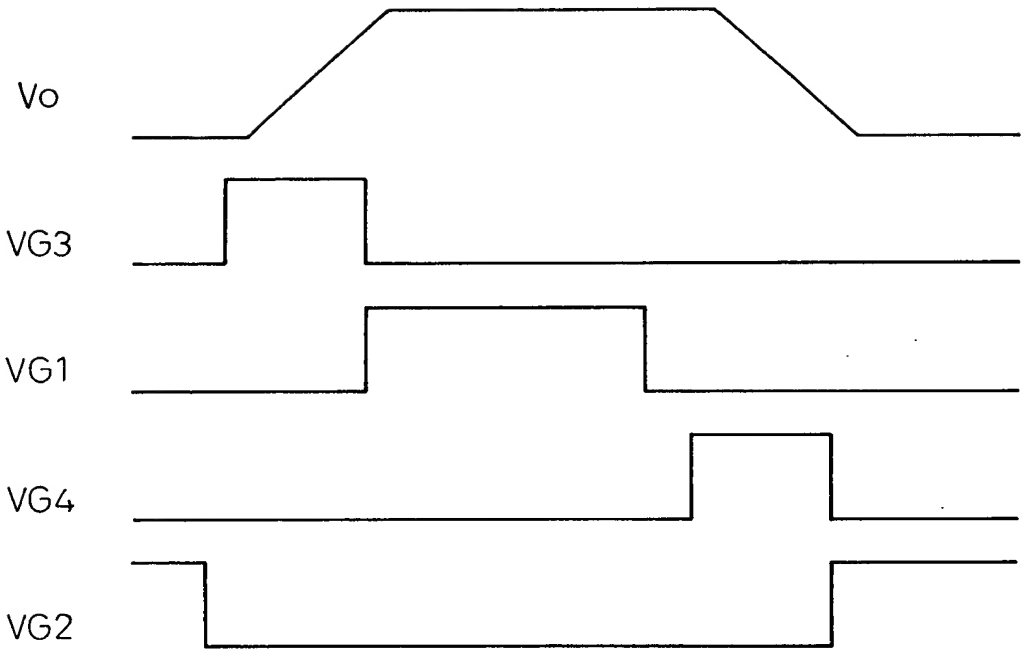


Fig.9

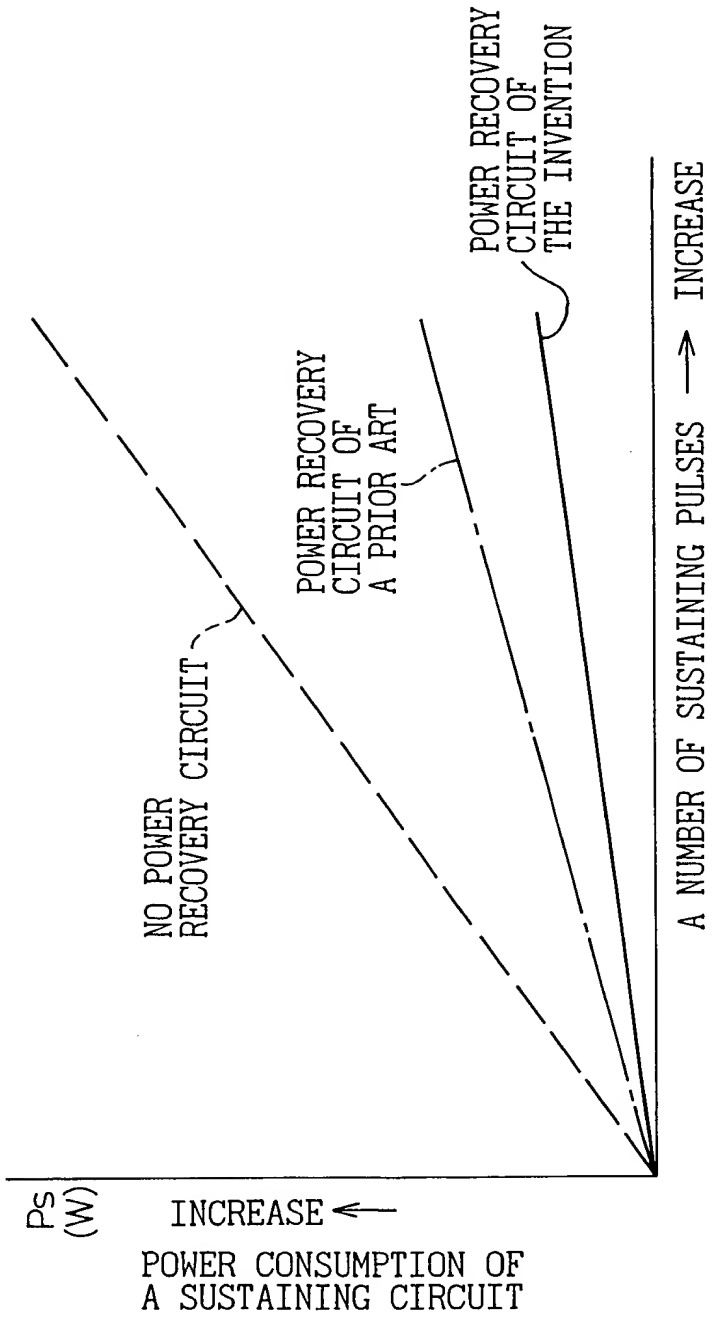

NO POWER RECOVERY CIRCUIT
POWER RECOVERY CIRCUIT OF A PRIOR ART
POWER RECOVERY CIRCUIT OF THE INVENTION
A NUMBER OF SUSTAINING PULSES → INCREASE
Ps (W)
INCREASE ←
POWER CONSUMPTION OF A SUSTAINING CIRCUIT

Fig.10

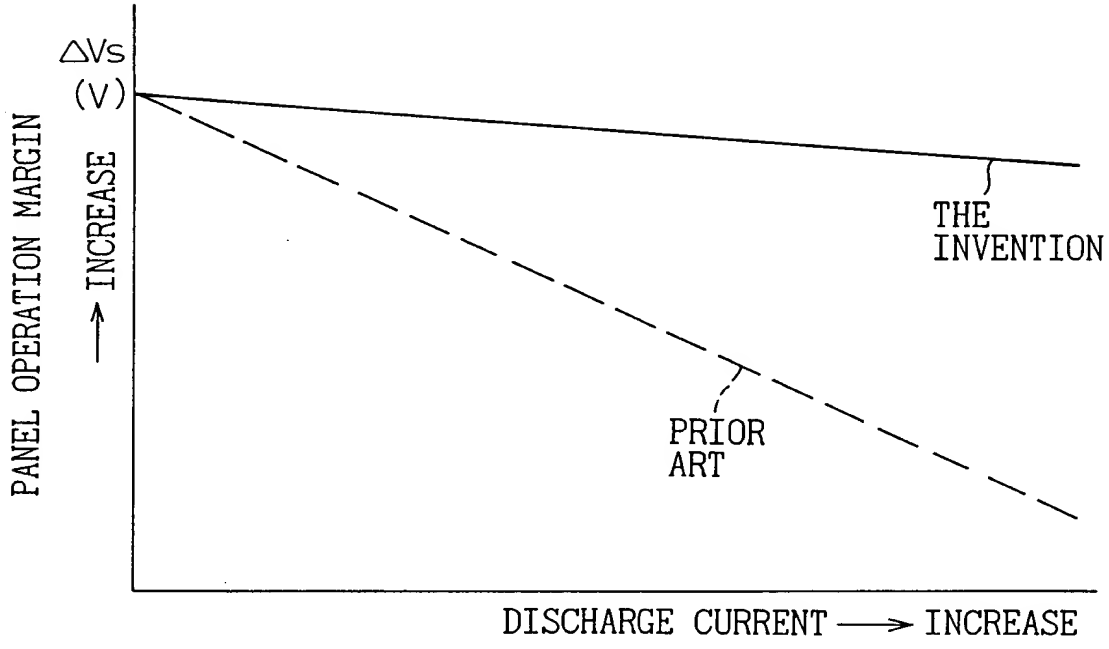

ΔVs
(V)
PANEL OPERATION MARGIN
INCREASE
THE
INVENTION
PRIOR
ART
DISCHARGE CURRENT → INCREASE

Fig.11A

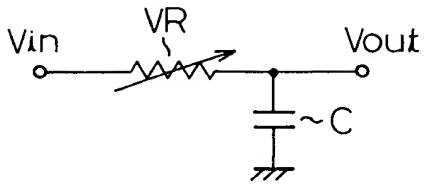


Fig.11B

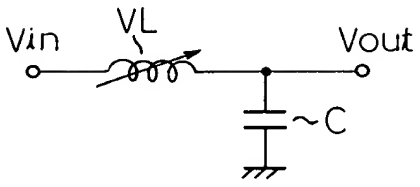


Fig.11C

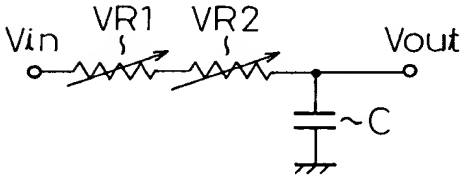


Fig.11D

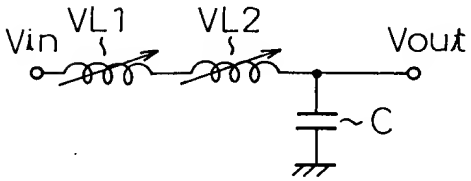


Fig.11E

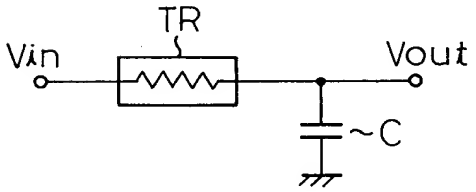


Fig.11F

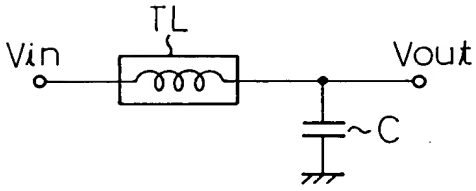


Fig.11G

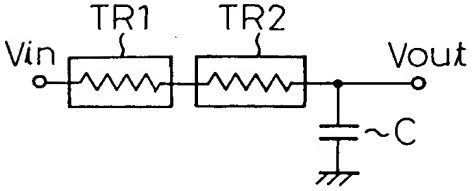


Fig.11H

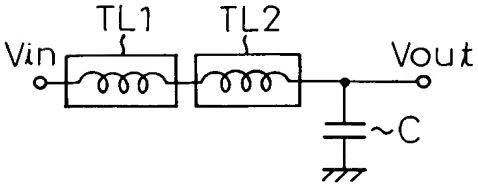


Fig.11I

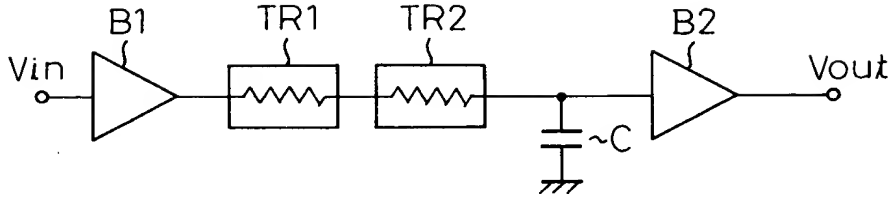


Fig.11J

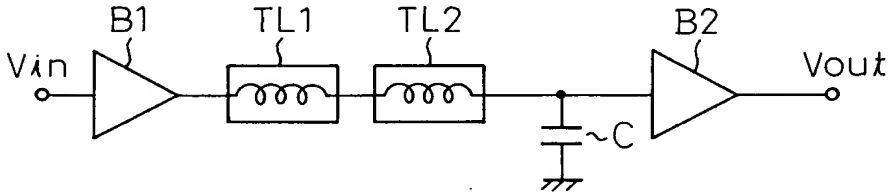


Fig.11K

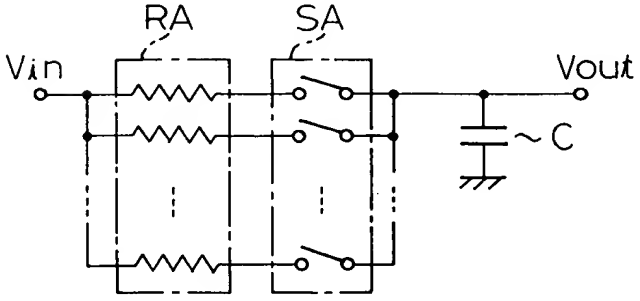


Fig.11L

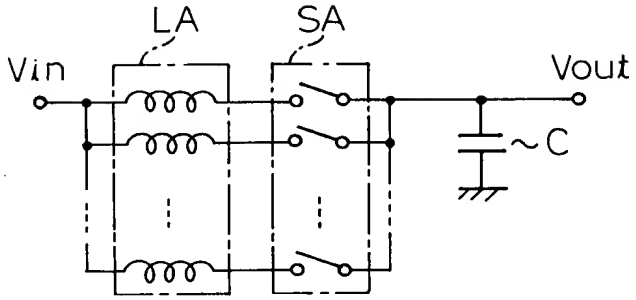


Fig.11M

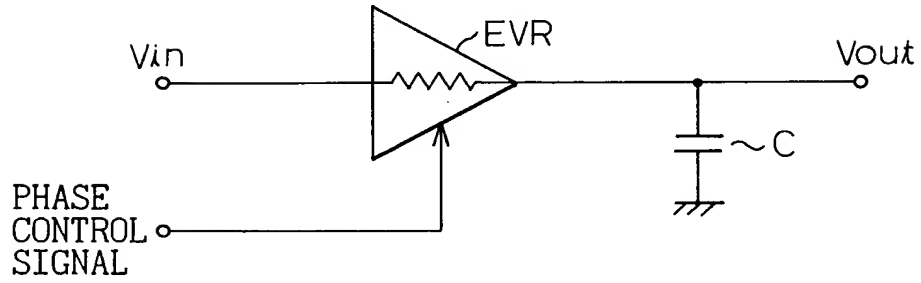


Fig.11N

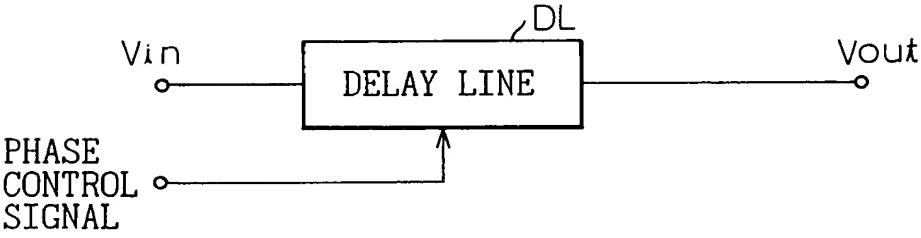


Fig.110

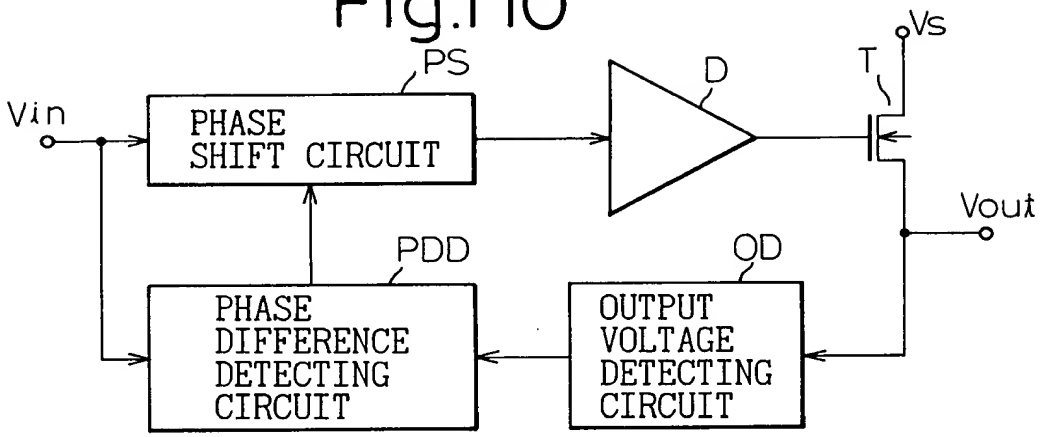


Fig.11P

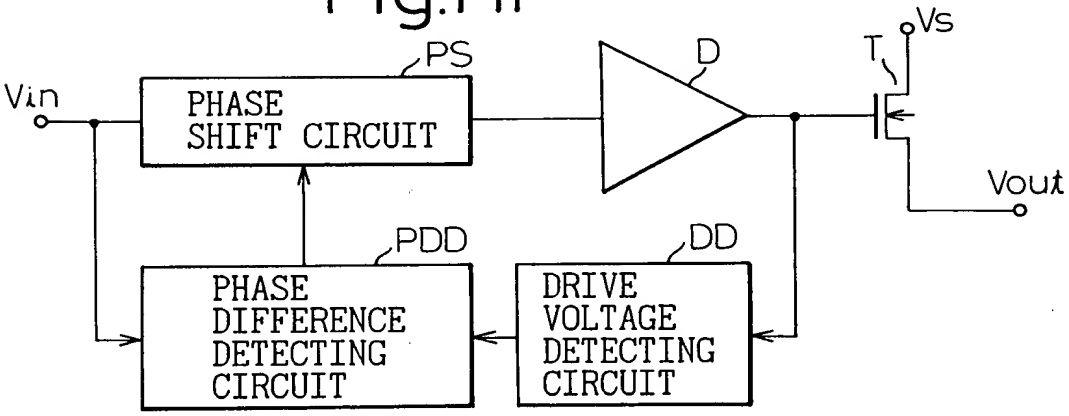


Fig.12

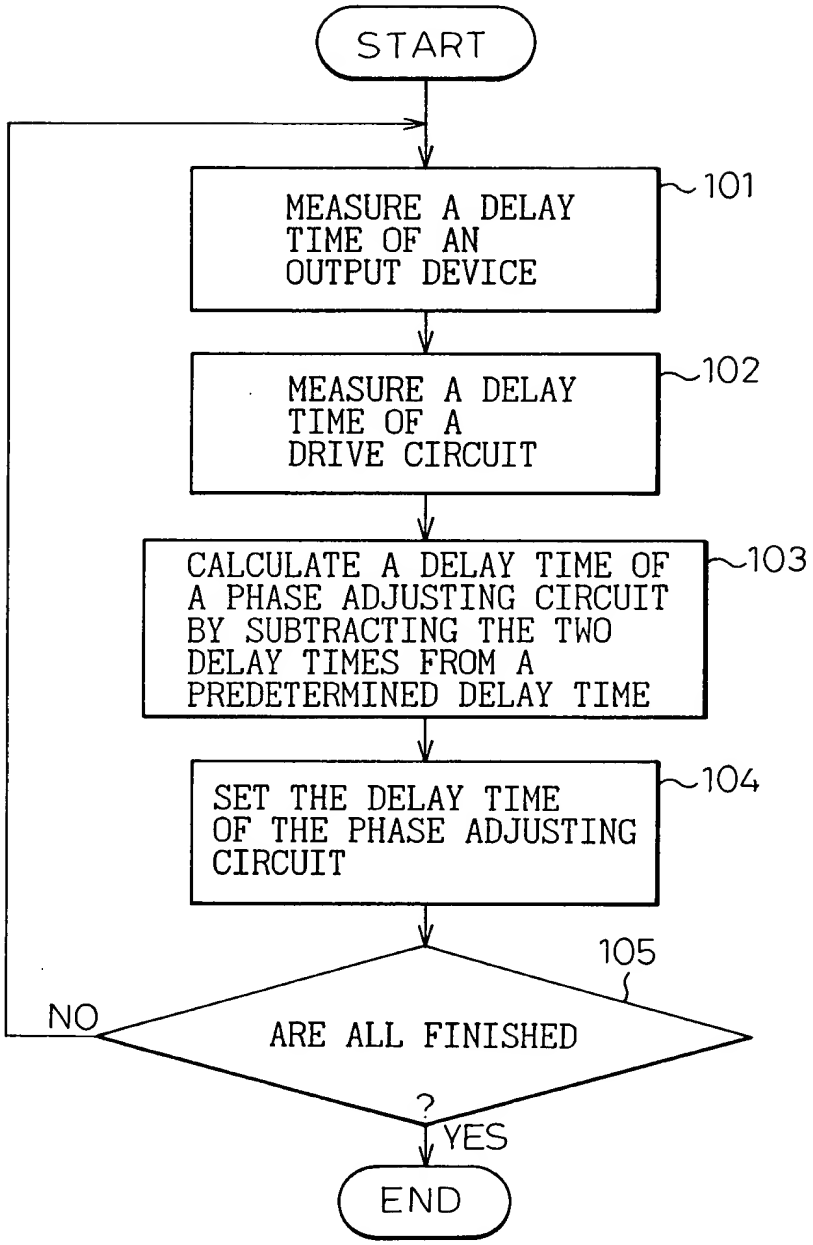

START
MEASURE A DELAY TIME OF AN OUTPUT DEVICE
101
MEASURE A DELAY TIME OF A DRIVE CIRCUIT
102
CALCULATE A DELAY TIME OF A PHASE ADJUSTING CIRCUIT BY SUBTRACTING THE TWO DELAY TIMES FROM A PREDETERMINED DELAY TIME
103
SET THE DELAY TIME OF THE PHASE ADJUSTING CIRCUIT
104
105
ARE ALL FINISHED ?
NO
YES
END

Fig.13

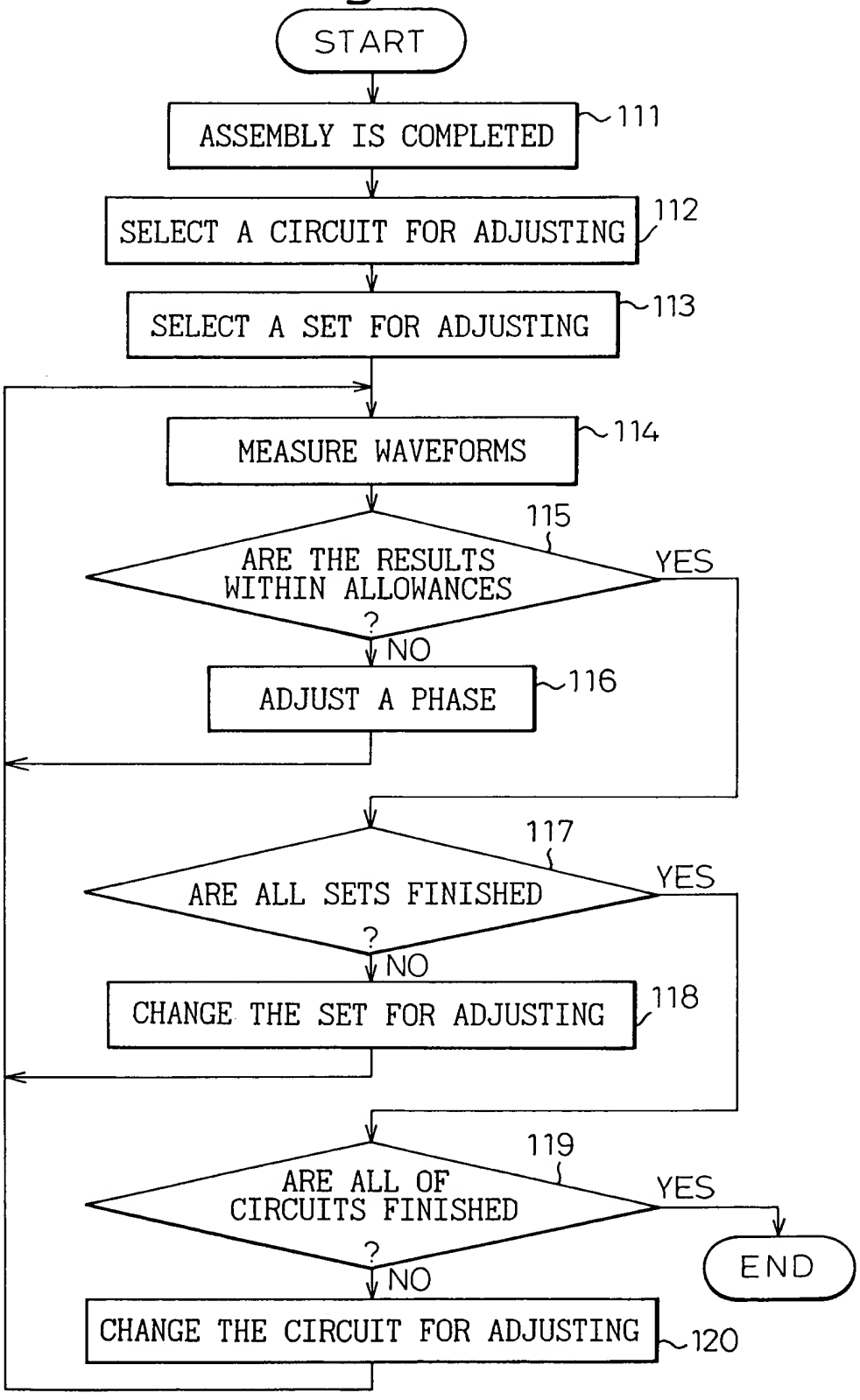

START
ASSEMBLY IS COMPLETED
111
SELECT A CIRCUIT FOR ADJUSTING
112
SELECT A SET FOR ADJUSTING
113
MEASURE WAVEFORMS
114
115
ARE THE RESULTS WITHIN ALLOWANCES ?
YES
NO
ADJUST A PHASE
116
117
ARE ALL SETS FINISHED ?
YES
NO
CHANGE THE SET FOR ADJUSTING
118
119
ARE ALL OF CIRCUITS FINISHED ?
YES
NO
END
CHANGE THE CIRCUIT FOR ADJUSTING
120

Fig.14

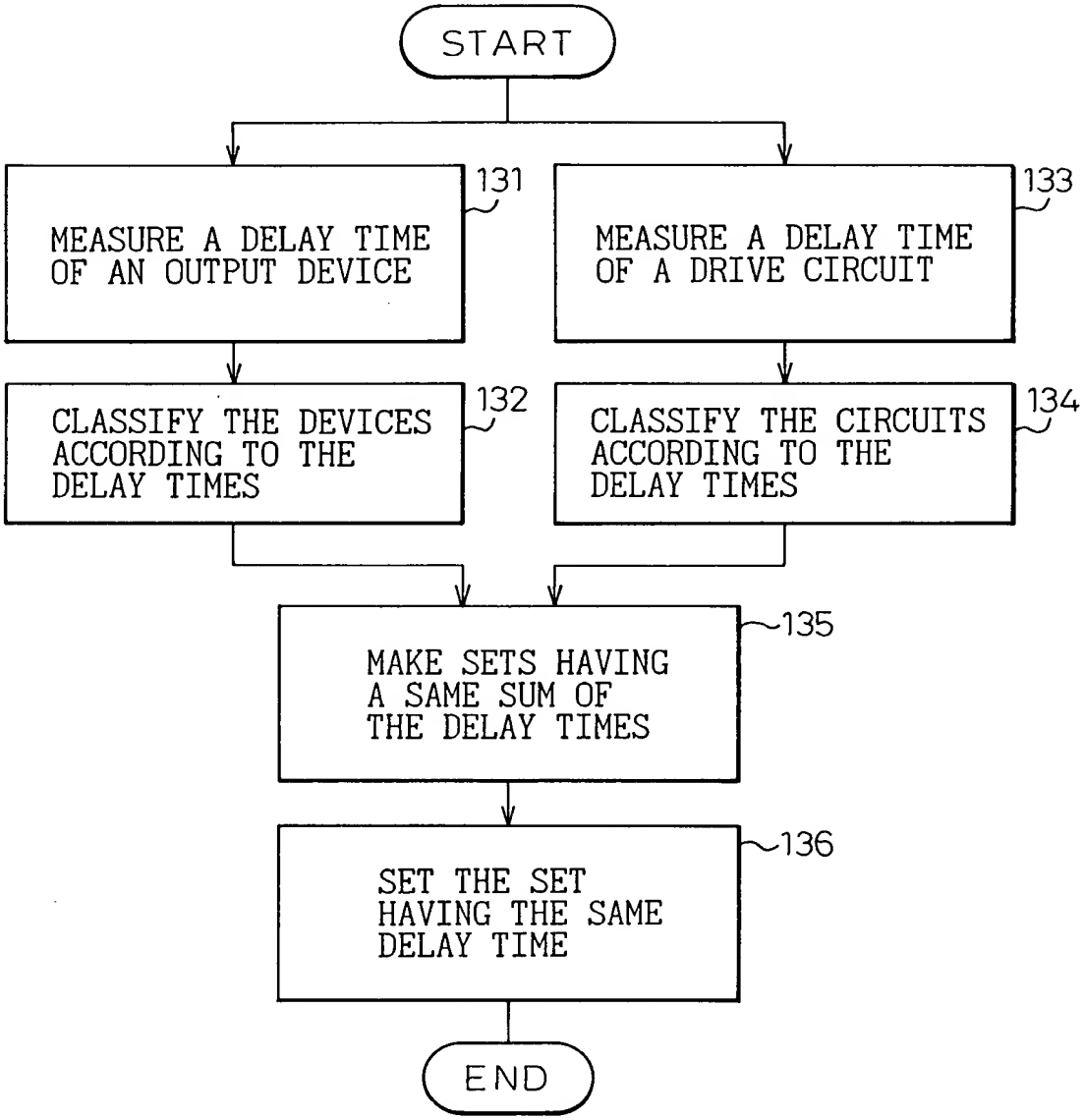

START
MEASURE A DELAY TIME OF AN OUTPUT DEVICE
131
MEASURE A DELAY TIME OF A DRIVE CIRCUIT
133
CLASSIFY THE DEVICES ACCORDING TO THE DELAY TIMES
132
CLASSIFY THE CIRCUITS ACCORDING TO THE DELAY TIMES
134
MAKE SETS HAVING A SAME SUM OF THE DELAY TIMES
135
SET THE SET HAVING THE SAME DELAY TIME
136
END

Fig.15

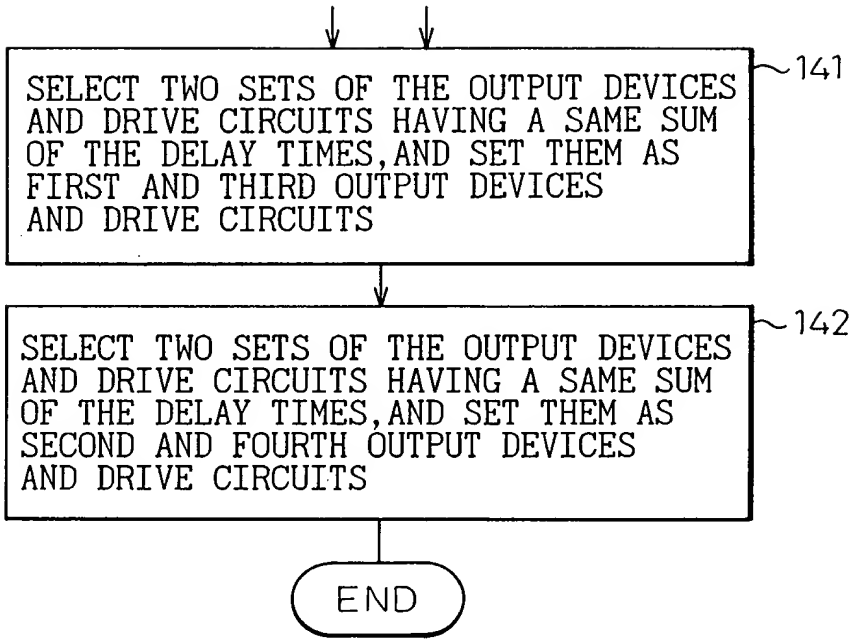
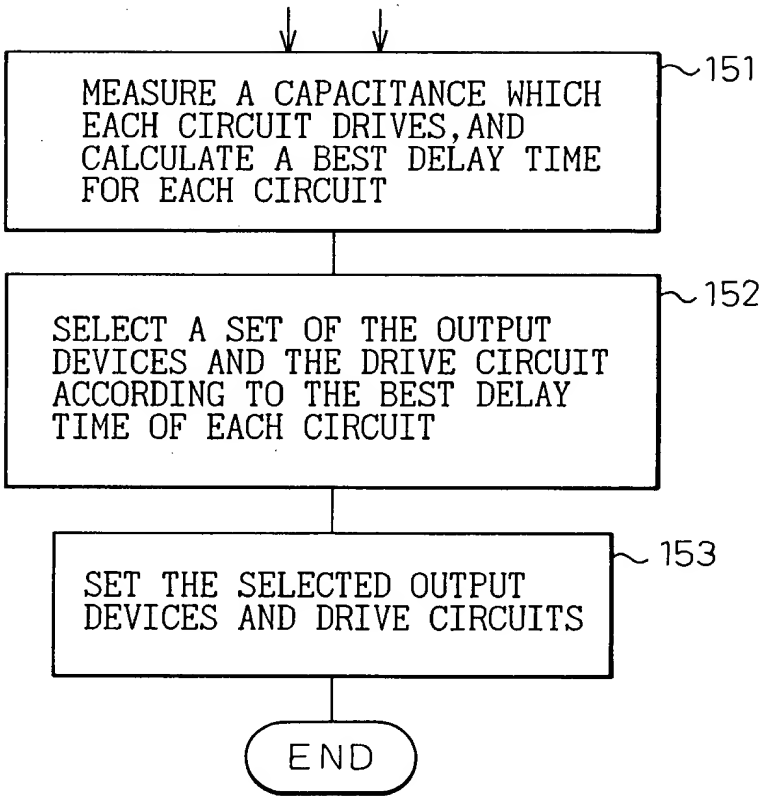

SELECT TWO SETS OF THE OUTPUT DEVICES AND DRIVE CIRCUITS HAVING A SAME SUM OF THE DELAY TIMES, AND SET THEM AS FIRST AND THIRD OUTPUT DEVICES AND DRIVE CIRCUITS
141
SELECT TWO SETS OF THE OUTPUT DEVICES AND DRIVE CIRCUITS HAVING A SAME SUM OF THE DELAY TIMES, AND SET THEM AS SECOND AND FOURTH OUTPUT DEVICES AND DRIVE CIRCUITS
142
END

Fig.16


MEASURE A CAPACITANCE WHICH EACH CIRCUIT DRIVES, AND CALCULATE A BEST DELAY TIME FOR EACH CIRCUIT
151
SELECT A SET OF THE OUTPUT DEVICES AND THE DRIVE CIRCUIT ACCORDING TO THE BEST DELAY TIME OF EACH CIRCUIT
152
SET THE SELECTED OUTPUT DEVICES AND DRIVE CIRCUITS
153
END